Enrollment No:-_____ Exam Seat No:-_____

C.U.SHAH UNIVERSITY

Summer-2015

Subject Code: **4TE03DCI1** Subject Name: Digital Circuits

Course Name: B.Tech Date: 6/5/2015

Semester: III Marks: 70

Time:02:30 TO 5:30

Instructions:

1) Attempt all Questions of both sections in same answer book/Supplementary.
2) Use of Programmable calculator & any other electronic instrument prohibited.
3) Instructions written on main answer book are strictly to be obeyed.
4) Draw neat diagrams & figures (if necessary) at right places.
5) Assume suitable & perfect data if needed.

SECTION – I

Q.1	(a)	Draw Symbol and Truth Table of AND Gate.	02
	(b)	Draw Symbol and Truth Table of OR Gate.	02
	(c)	Draw Symbol and Truth Table of NOR Gate.	02
	(d)	Draw Symbol and Truth Table of NOT Gate.	01
Q.2	(a)	Explain with figures how NAND gate and NOR gate can be used as Universal gate.	05
	(b)	Explain and compare 1's complement and 2's complement.	05
	(c)	Find 9's complement of (a) 3465 (b) 782.54.	04
		OR	
Q.2	(a)	Explain 4 bit reflected code.	05
	(b)	Explain Excess-3 code and generate Excess-3 code for numbers 0-9.	05
	(c)	Convert Binary to Octal (a) 110101.101010 (b)10101111001.0111.	04
Q.3	(a)	Simplify F(w,x,y,z) = $\Sigma(1,3,7,11,15)$ and don't care d(w,x,y,z) = $\Sigma(0,2,5)$.	05
	(b)	Simplified expression in (a)sum of products and (b) product of sum: F(A,B,C,D) = $\Sigma(0,1,2,5,8,9,10)$.	05
	(c)	Prove that $m_j' = M_j$.	04
Q.3	(a)	Design a combination circuits for a full adder.	05
	(b)	Design a combination circuits for a full substractor.	05
	(c)	Simplify F= A'C + A'B +AB'C + BC.	04

SECTION – II

Q.4	(a)	Draw Symbol and Truth Table of NAND Gate.	02
	(b)	Draw Symbol and Truth Table of XOR Gate.	02
	(c)	Draw Symbol and Truth Table of XNORGate.	02
	(d)	What is Byte?	01
Q.5	(a)	Explain the working of the Master Slave J K flip-flop.	05
	(b)	Explain the working of the S R flip-flop.	05
	(c)	Design and implement BCD to excess 3 code converter using 4 bit full adder.	04

OR

Q.5	(a)	Explain 3 to 8 line decoder.	05
	(b)	Implement a full adder using 3 to 8 line decoder and two OR gates.	05
	(c)	Write a short note on demultiplexer.	04
Q.6	(a)	Design Octal to Binary encoder.	05
	(b)	Implement F (A, B, C, D) = Σ (1, 3, 5, 6) with a multiplexer.	05
	(c)	Explain T flip-flop.	04

OR

Q.6	(a)	Write a short note on Register.	05
	(b)	Explain Binary ripple counter.	05
	(c)	Compare Sequential and Combinational logic circuit.	04